WHAT IS CLAIMED IS:

1. A data processor comprising:

a central processing unit; and

a memory card interface controller connectable to a clock synchronized memory card,

wherein said memory card interface controller transmits a clock signal to said memory card to acquire read data therefrom in synchronism with said clock signal, said memory card interface controller being switchable between a raising edge and a falling edge of said clock signal when acquiring said read data in synchronous relation with said clock signal.

2. A data processor according to claim 1, wherein said memory card interface controller is switchable between different frequencies of said clock signal.

3. A data processor according to claim 1, wherein said central processing unit switches between the raising edge and the falling edge of the clock signal in response to a data read error during read data acquisition in synchronism with the clock signal.

4. A data processor according to claim 2, wherein said central processing unit switches from a high fre-

quency to a low frequency of the clock signal in response to a data read error.

5. A data processor according to claim 2, wherein said central processing unit switches between the raising edge and the falling edge of the clock signal in response to a data read error during read data acquisition in synchronism with said clock signal, the central processing unit further switching from a high frequency to a low frequency of the clock signal in response to a data read error following the switching between the raising edge and the falling edge of the clock signal.

6. A data processor according to claim 1, wherein said central processing unit switches from a high frequency to a low frequency of the clock signal in response to a data read error, said central processing unit further switching between the raising edge and the falling edge of the clock signal in response to a data read error after the frequency switching during read data acquisition in synchronism with the clock signal.

7. A data processor according to claim 1, further comprising:

a first register accessible by said central proc-

essing unit, the first register being loaded with control data for determining whether said read data is to be acquired in synchronism with the raising edge or with the falling edge of said clock signal.

8. A data processor according to claim 2, further comprising:

first and second registers accessible by said central processing unit, said first register being loaded with control data for determining whether said read data is to be acquired in synchronism with the raising edge or with the falling edge of said clock signal, said second register being loaded with control data for determining whether said clock signal is to have a high frequency or a low frequency.

9. A data processor according to claim 8, further comprising:

a nonvolatile memory which is electrically rewritable and which serves as a storage area for accommodating a control program executed by said central processing unit in order to generate said control data.

10. A data processor according to claim 1, wherein said memory card interface controller transmits data

to said memory card in synchronism with the clock signal, said memory card interface controller being switchable between the raising edge and the falling edge of said clock signal when transmitting the data in synchronous relation with said clock signal.

11. A memory card for receiving a clock signal from a memory card host device and transmitting read data to said memory card host device,

wherein said memory card determines whether to synchronize with a raising edge or with a falling edge of said clock signal when transmitting said read data.

12. A memory card according to claim 11, wherein said memory card host device instructs said memory card to determine whether to synchronize with the raising edge or with the falling edge of said clock signal.

13. A memory card according to claim 11, wherein said memory card acquires data from the memory card host device in synchronism with said clock signal, said memory card further determining whether to synchronize with the raising edge or with the falling edge of said clock signal when acquiring said data.